Enabling Co-Design of Systems and Packages

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Cadence Design Systems

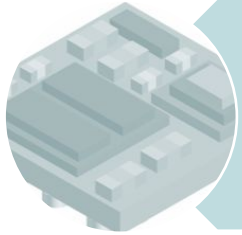
Outline

- Trends
- Challenges
- Solutions
- Conclusion

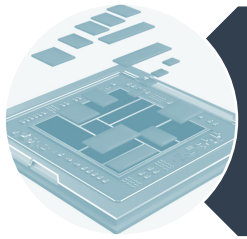
The Beginning of the “More Than Moore” Era

For the past five decades, the electronic industry has thrived while enjoying the benefits of Moore’s Law. But things are changing…The economics of semiconductor logic scaling are gone…

Gordon Moore knew this day would come. He also predicted that *”It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.”*



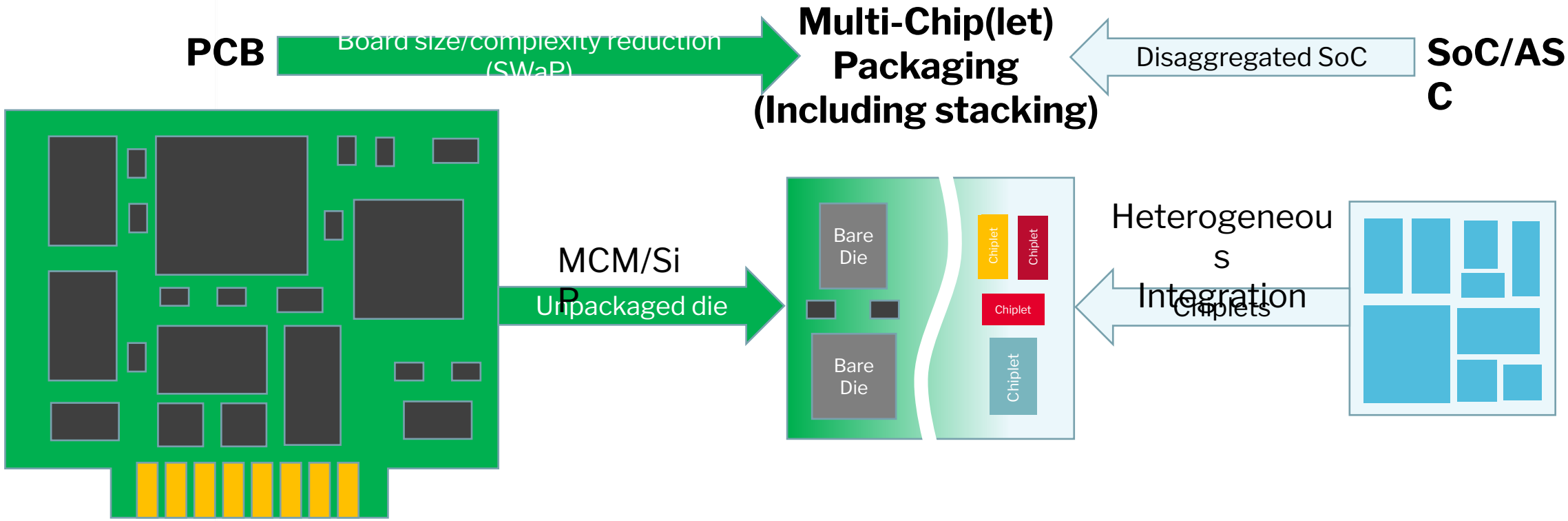
Co-Designing Systems with Boards, multi-chiplet SiPs have become necessary for cost-sensitive complex designs



The generation of “More Than Moore” is here…

The **WHAT** of Chiplets

The transition from system on a chip (SoC) to system in a package (SiP)



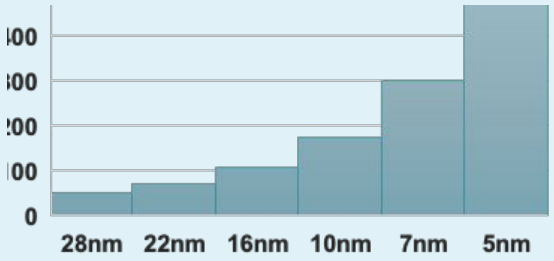
PCB to MCM/SiP Benefits
Smaller footprint
PCB simplification
Higher bandwidth
Lower power

SoC to HI Benefits
Reduced NRE costs
Shorter time to market
Larger than reticle size designs
More flexible IP use-model

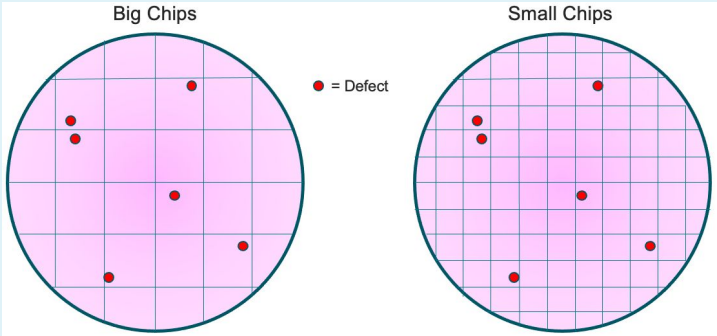
The **WHY** of Chiplets

Following Moore's Law alone no longer the best technical and economical path forward

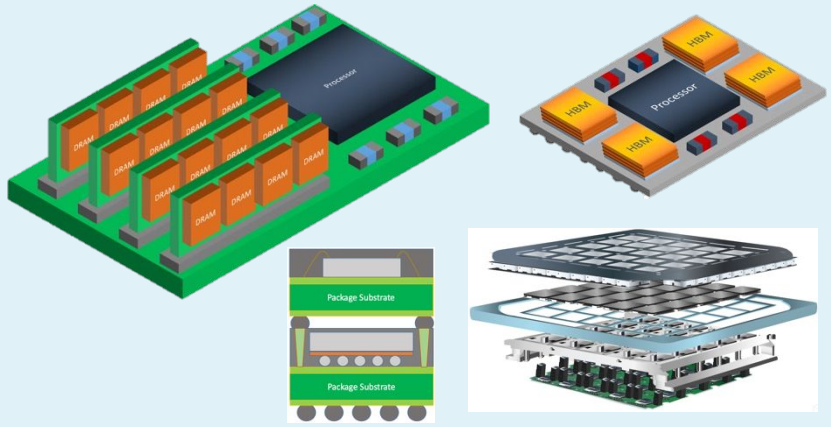
Cost



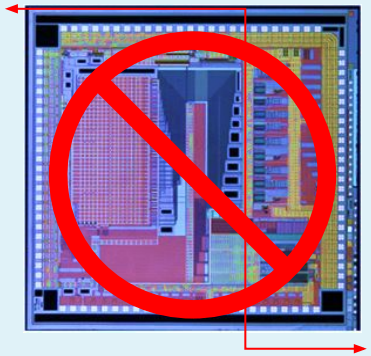
Yield



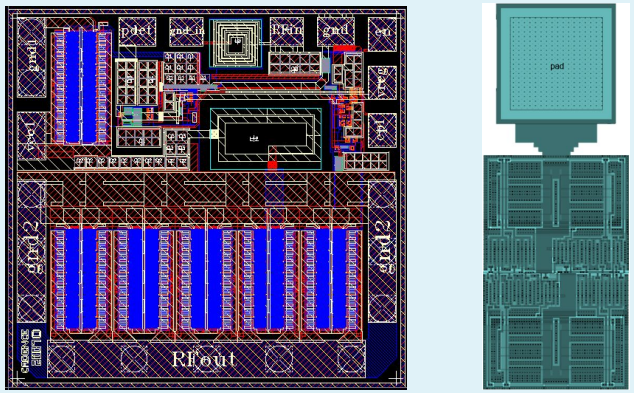
Memory Bandwidth



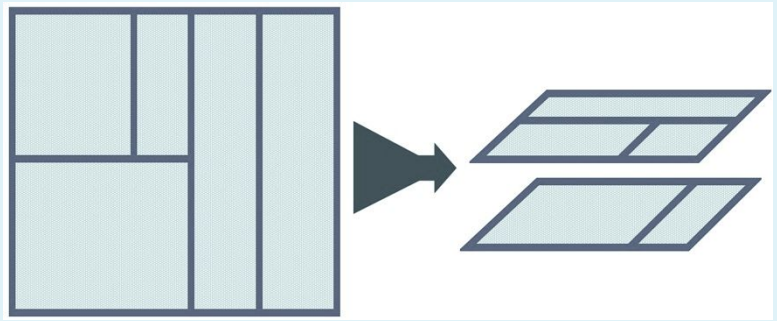
Size



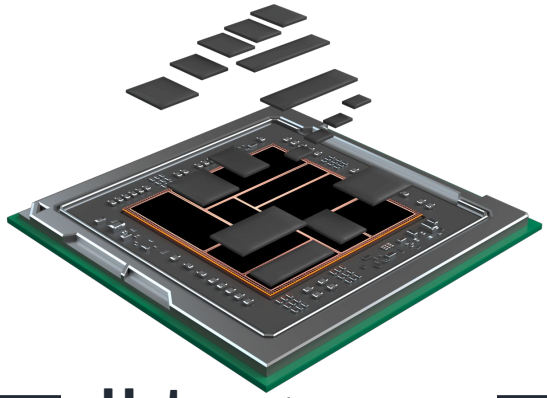
Analog/RF and I/O



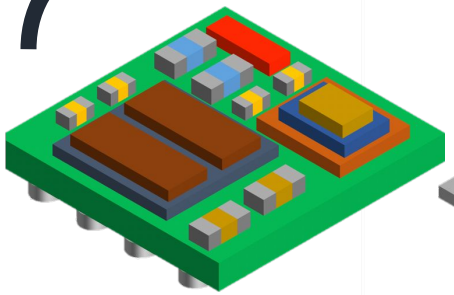
Form-Factor and Modularization



Technology Breakthroughs in Semiconductor Packaging

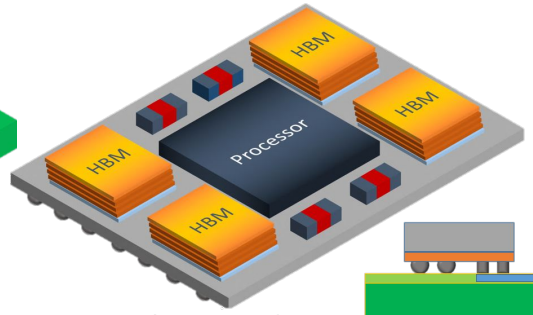


Heterogeneous Integration (Chiplets)



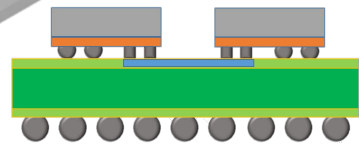
System in Package (SiP/MCM)

1990



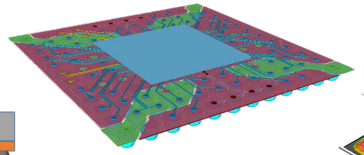
2.5D-IC (Silicon/RDL Interposer)

2010



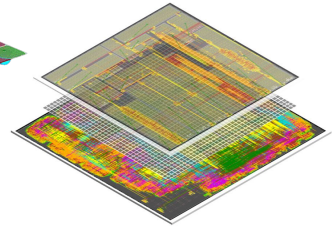
Interconnect Bridges

2012



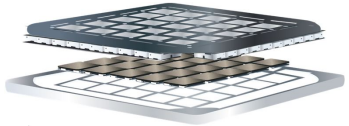
Ultra-High-Density RDL (FO/WLP)

2015



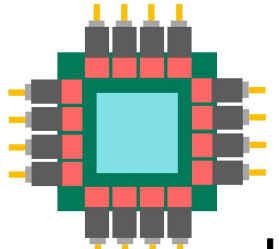
Silicon Stacking

2018



3D System-on-a-Wafer

2020



Optics

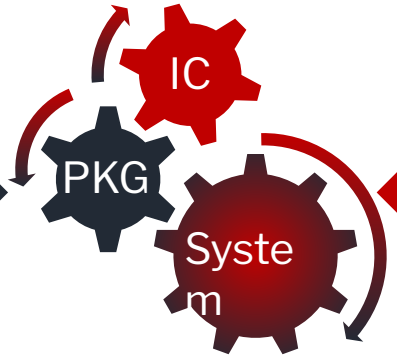
2022

The Needs of IC and Systems Designers are Converging

OSATs (SWaP)

Board design impact on packaging

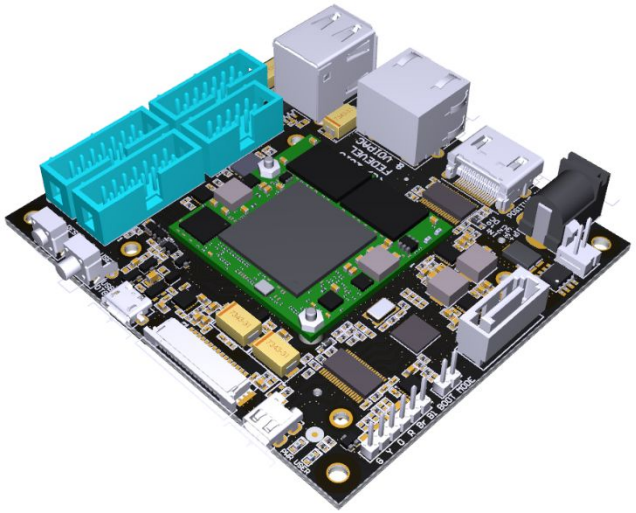
1980-2010



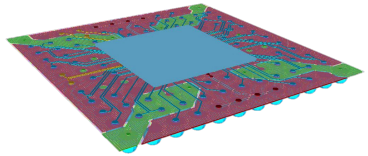
Foundries (PPA)

IC design impact on packaging

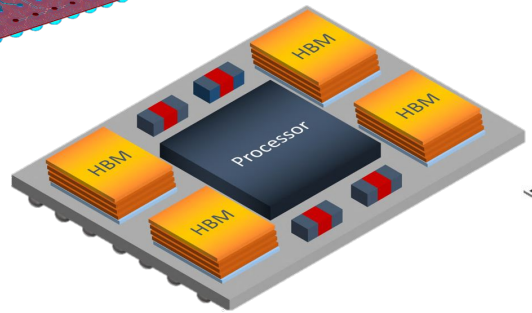
2011-Now

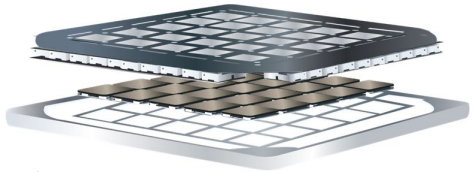


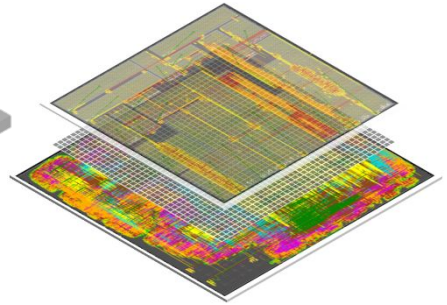
PCB Layout Flow
System-Level Analysis



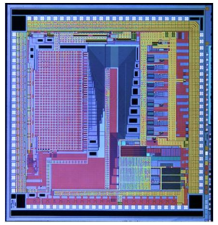
PCB-like Flow
System-Level Analysis





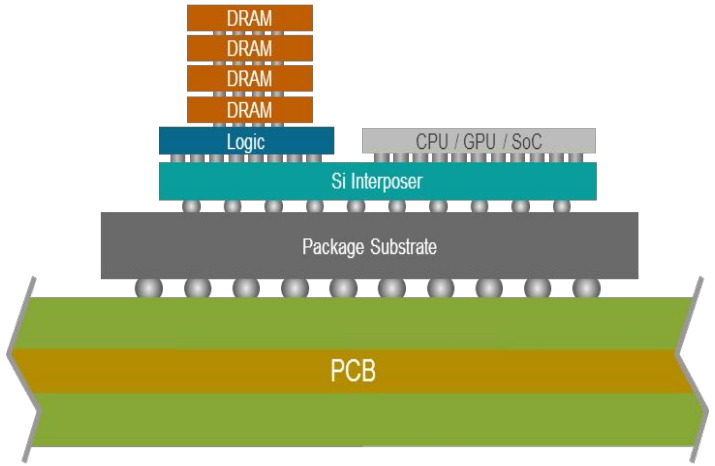


IC-like Implementation Flow
IC signoff Methodology and
System-Level Analysis



IC Flow
IC signoff
Methodology

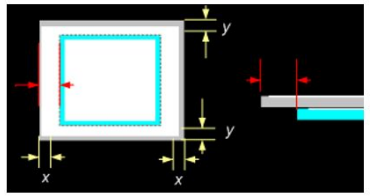
Times Have Changed…



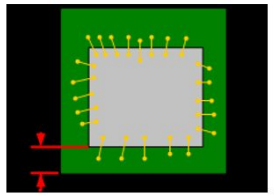
- Yesterdays Advanced IC Packaging
  - *Necessary evil*
  - Avoid negative impact on chip
    - Electrical, Thermal
  - Protect chip from the outside world
  - Redistribute IO to pitch more suitable for the PCB layout

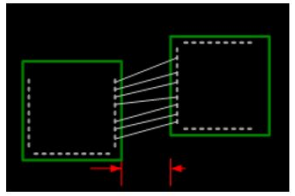
- Todays advanced IC packaging is about *adding value* to end products
  - Companies leveraging packaging technologies to create value and differentiation from their competitors
  - TSV, WLP and 3D stacking technologies providing a tremendous number of packaging options for all form-factors and budgets
  - Optimizing packaging with IC, Chiplets and PCBs is **not optional anymore**.
  - **Optimizing package parameters for best PPA**

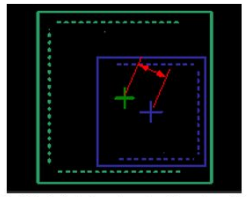
Multi-Chiplet Ecosystem Challenges

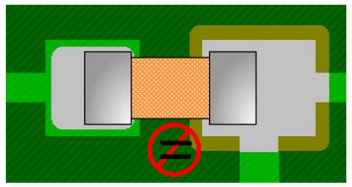


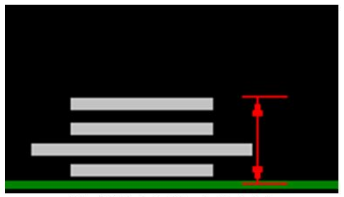
Die/Chiplet Overhang

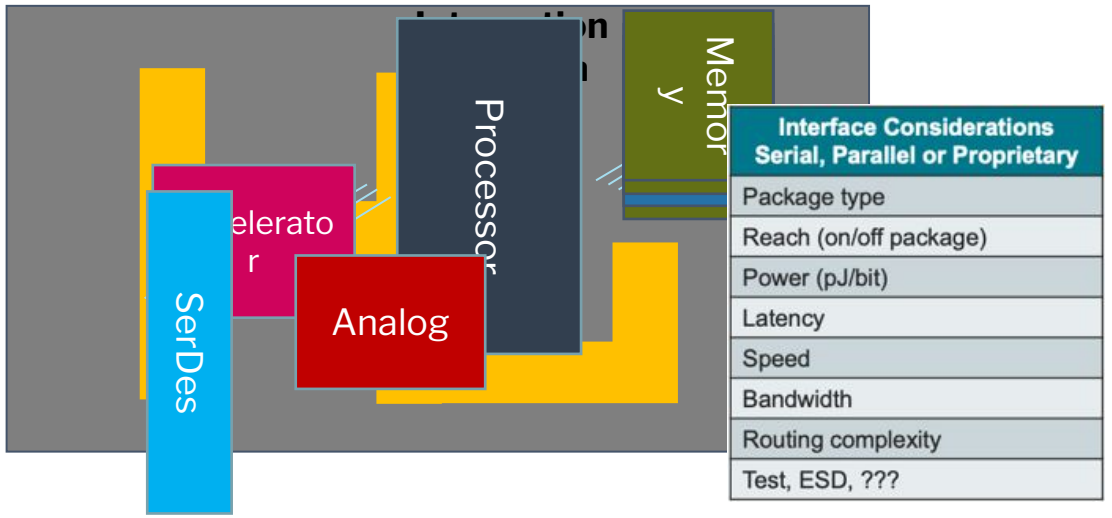

Die/Chiplet Spacing to Substrate Edge


Die/Chiplet to Die/Chiplet Spacing


Die/Chiplet Center to Center Offset


Tombstone Effect (% size diff)


Die/Chiplet Stack Height



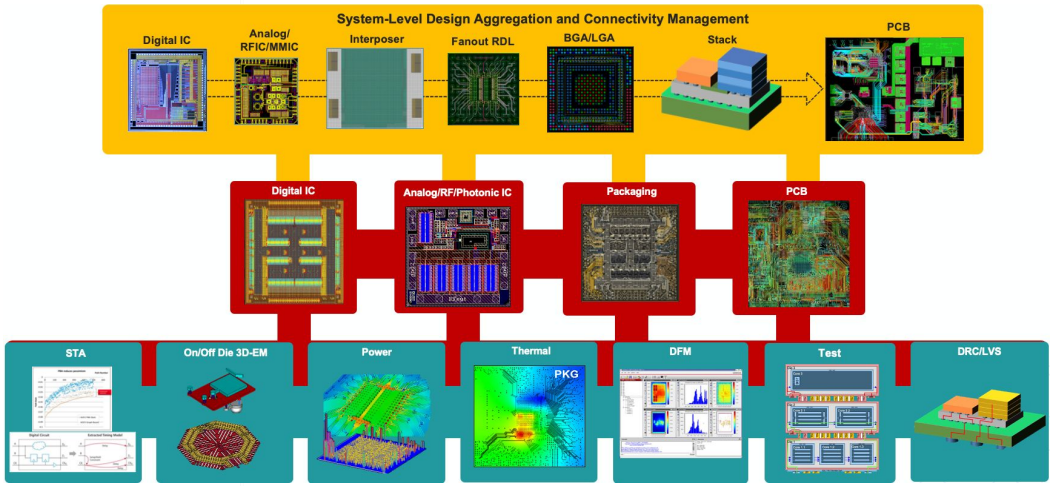
Assembly Design Kits

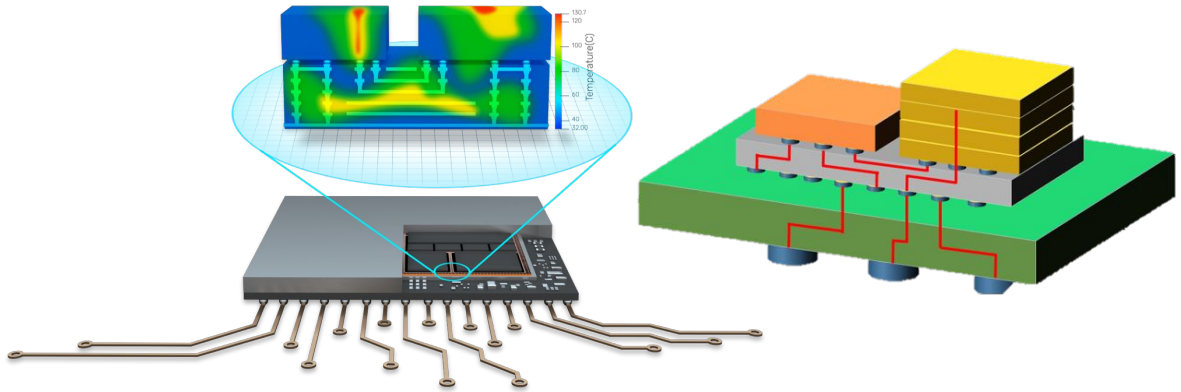
- PDK equivalent for the entire multi-chiplet assembly
- Historically, OSATs have not provided sufficient data to package designers
- Foundries need to provide the packaging engineer all the data he/she needs to produce manufacturing output of a design that can be assembled and tested
- Contents; tech files, libraries, assembly rules, substrate DFM, rule decks, and design templates
- Security and Test solutions

COTS Chiplets

- Most chiplet-based designs are in a closed ecosystem
- Business case for IP companies to provide 3rd type of IP
  - CHIPLET.US
- Progress with chiplet exchange formats
  - CDX, 3Dblox™,3DCODE
- Common communication interface
  - AIB, UCIe, BoW, …
  - Too many packaging options to standardize on a single interface

Multi-Chiplet Flow Challenges





Design Tools/Flows

- Explosion in the number of design tools and required expertise mean complex design flows
- **Co-design/co-analysis across die/chiplet/package is now mandatory**
- Capacity and performance impact on tools
- Support of existing and emerging 3D-IC standards
- Silicon stacking breaks abstract die representation use model
- Package designers pivoting to foundry-based design and sign-off requirements

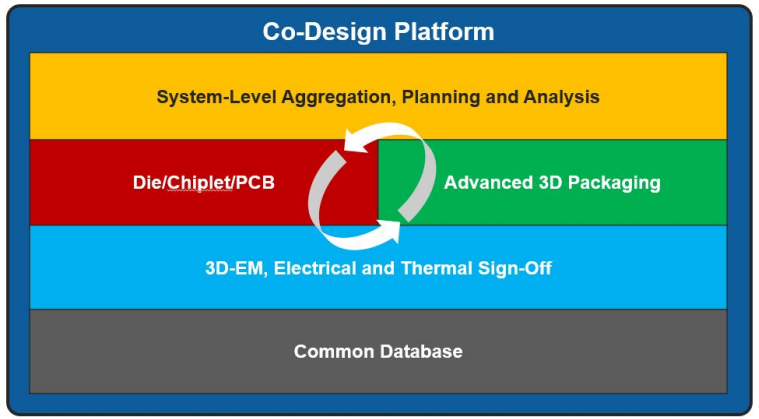
Analysis and Sign-Off

- Early-stage and signoff-level thermal/power analysis
- STA with automated corner reduction
- SystemLVS with rule-deck-free methodology
- Stacked-die EMIR
- Stress and CMP planarity checks
- New 3D-IC test standards
- High-capacity EM/SI/PI to support very large structures (billions of instances)
- Compliance kits for new chiplet-to-chiplet communication standards

Co-Optimization Enabling Platform

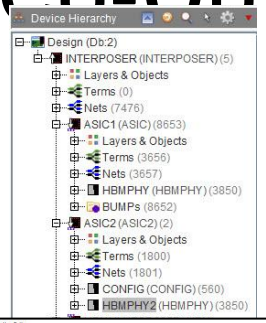
Integrated to Co-Analyze and Co-Optimize

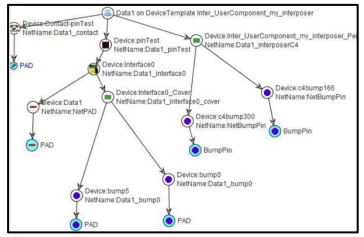
- Two or more systems often required to create optimal design
- Cross-platform solutions improve domain to domain data exchange/ co-design

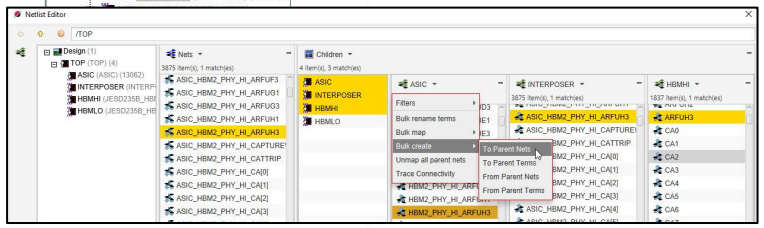


	Package/PCB	Analog/RF IC	Digital IC
Architecture	GUI-centric layout	Schematic capture, hierarchical layout	Language-driven flat design
Package Type	BGA/LGA, FOWLP, PoP, Si bridges	RF module, Photonics	2.5D-IC, 3D-IC
Die Model	Blackbox abstract	Transistor level	Standard Cell level
Routing Styles	Constraint-driven, push/shove 45-degree/ **any angle** routing	PDK-driven, 90/45 degree/CurvyCore™ routing	Timing-driven routing, 45-degree RDL routing
Extraction/ Analysis	3D-EM, SI and PI	RC Extraction + 3D-EM	RC Extraction
Manufacturing Outputs	Board/Substrate Foundry	Foundry	Foundry
Physical Verification	Only required in some applications	Sign-Off DRC and LVS	
OS	Windows, Linux	Linux	Linux

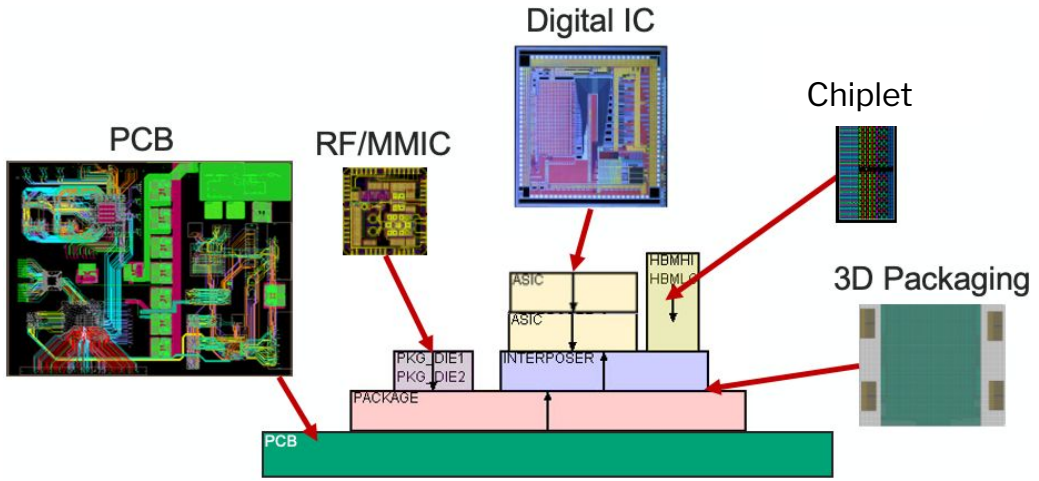
Top-Level Aggregation, Co-Planning, Co-Design and Co-Optimization



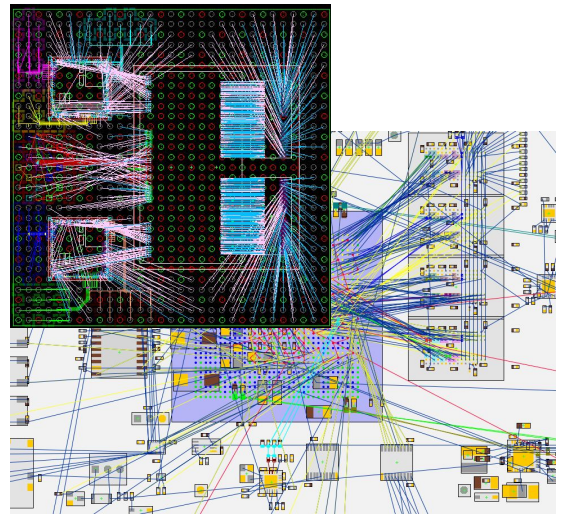




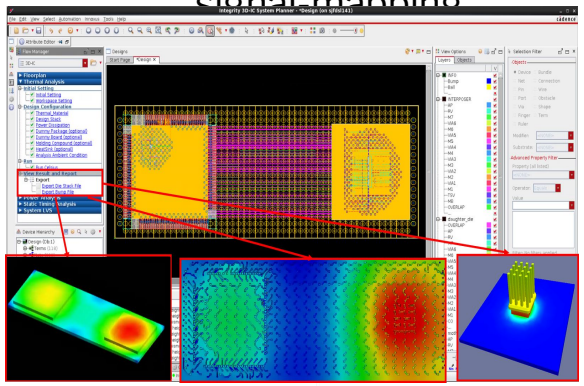
Multi-design management with chip(let)-chip(let)-package-board signal mapping



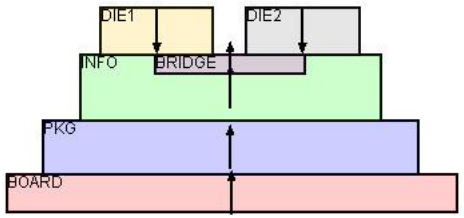
Hierarchical Planning and Optimization of System-Level Design and Connectivity



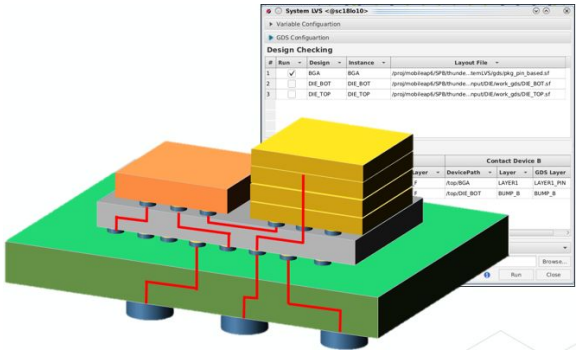
System-level co-optimization



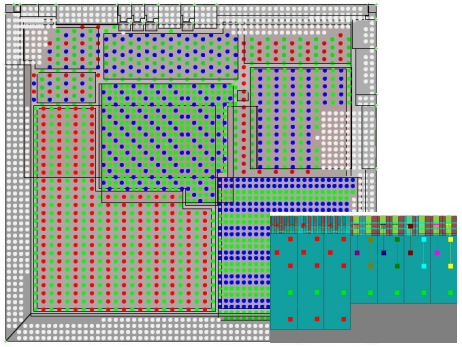
Early-Stage Thermal/Power Analysis



Stack management (Supports 3Dblox™)



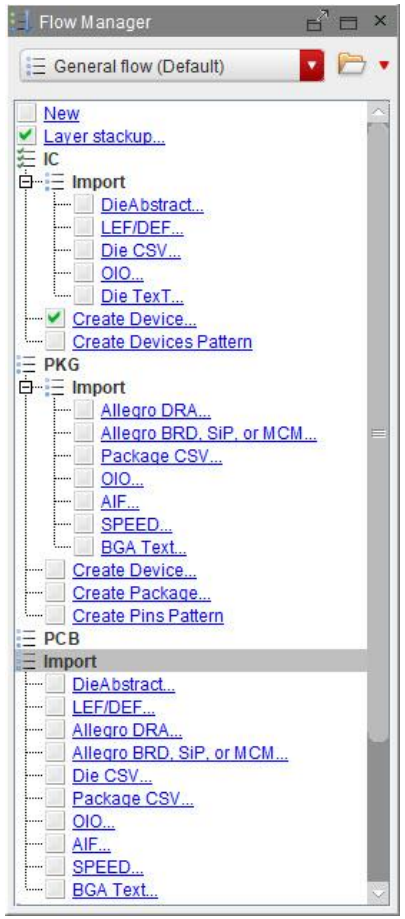
System-level connectivity/stack alignment verification (SystemLVS)



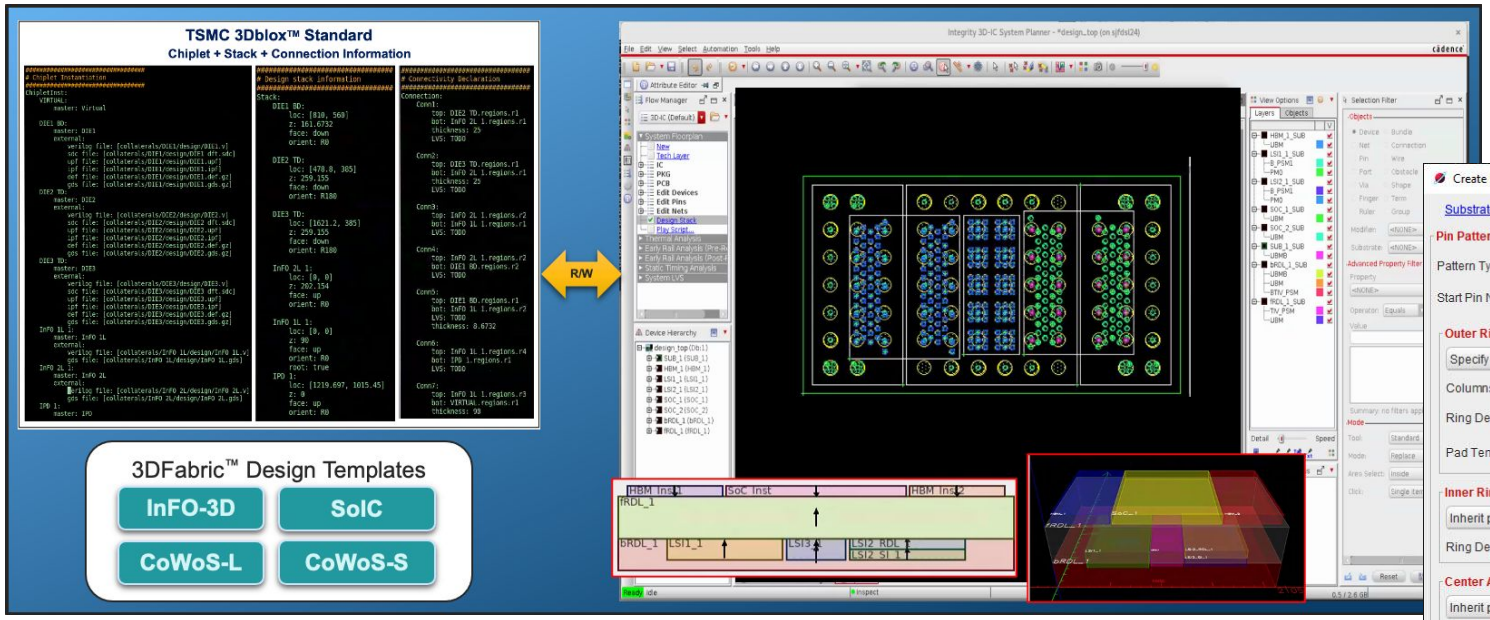
Advanced bump/TSV planning

Importing Design Data Into Co-Design Platform

Muti-source Inputs

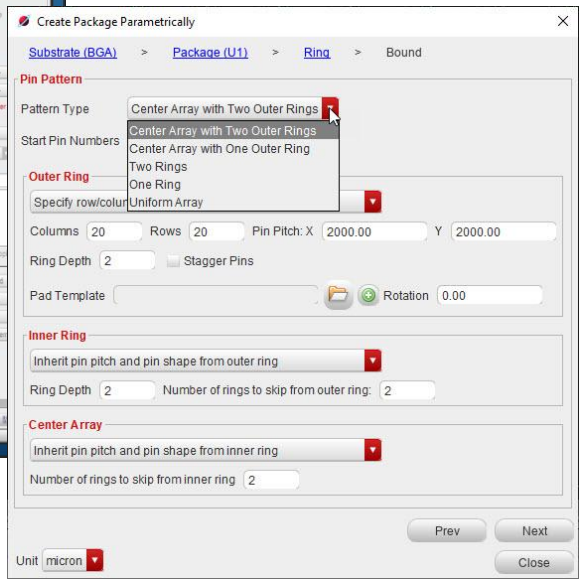


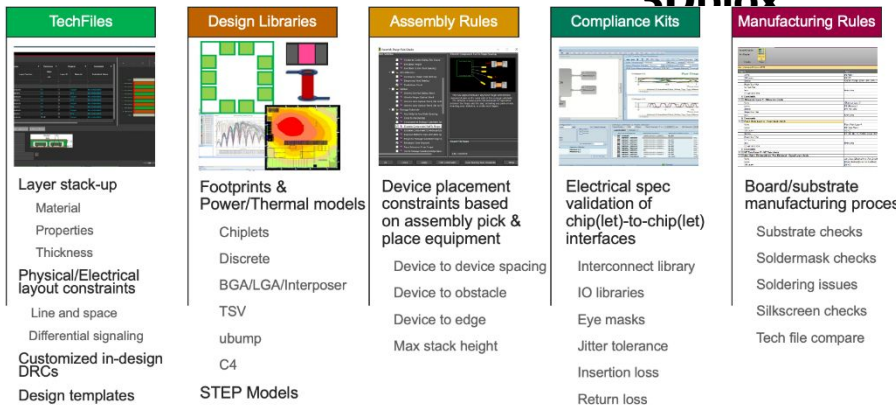
Industry Standard Formats



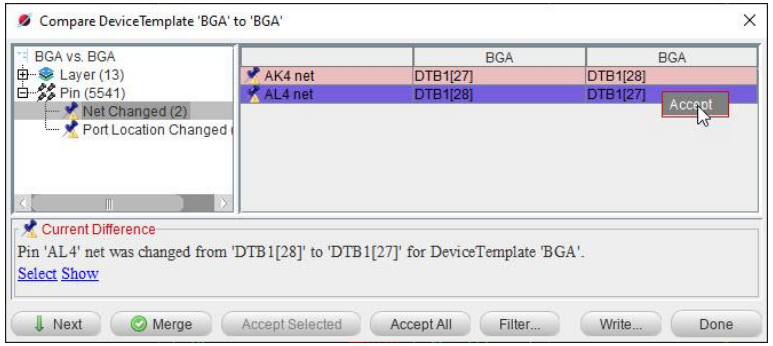
TSMC 3Dblox™

Build On-The-Fly



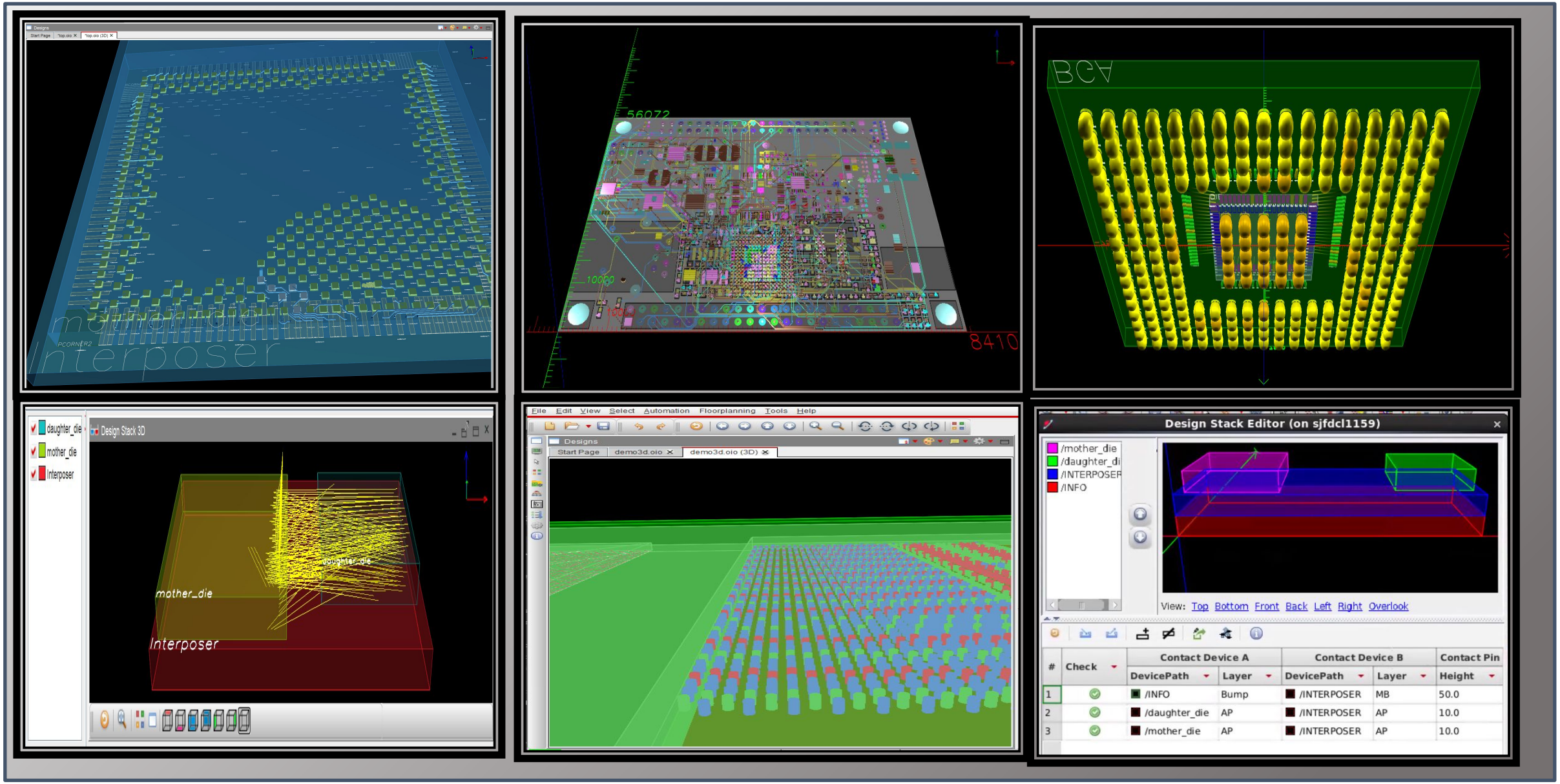


Assembly Design Kits (ADK)

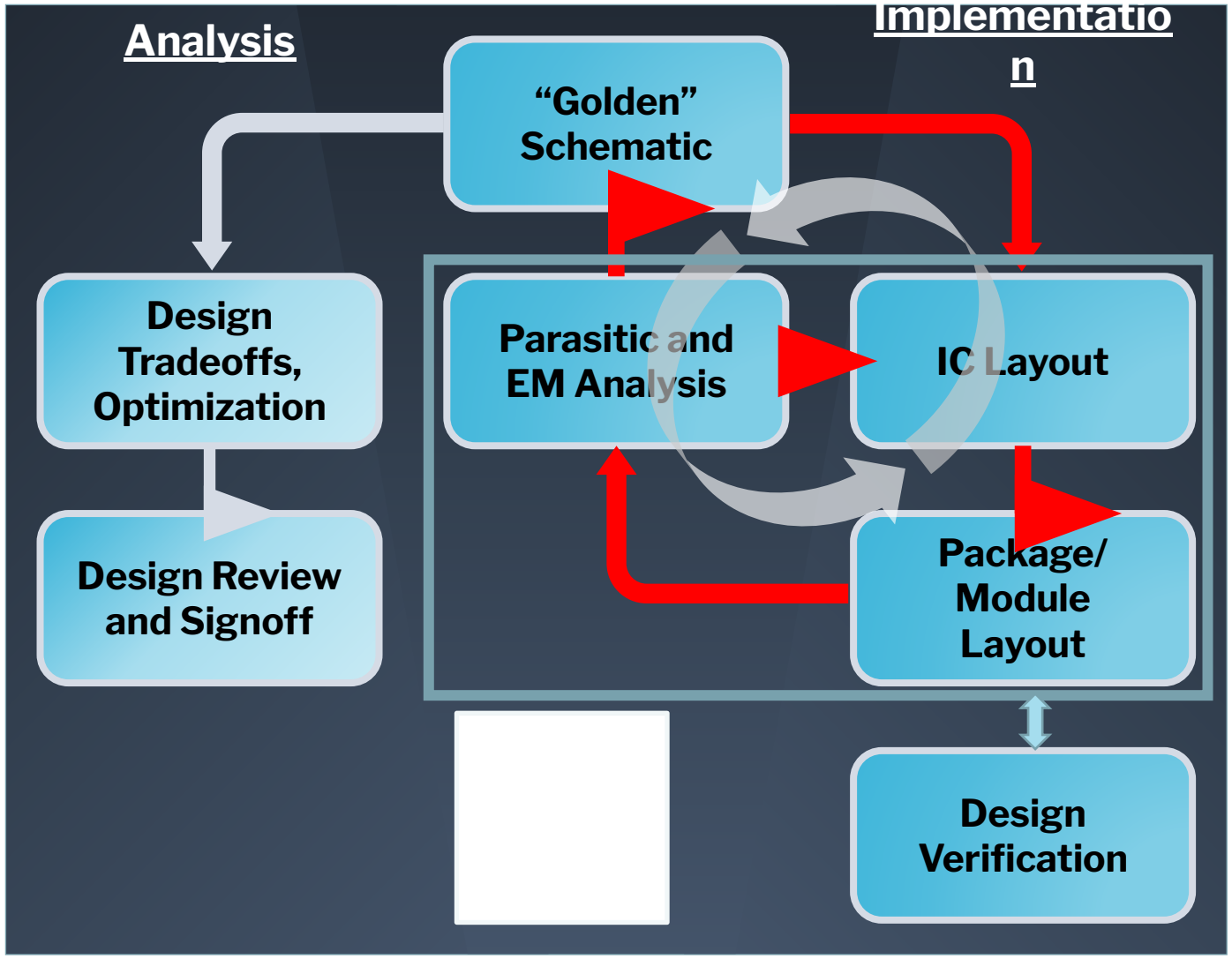


ECO Flow With Layout Tools

3D Viewing/Analysis/Checking/Editing



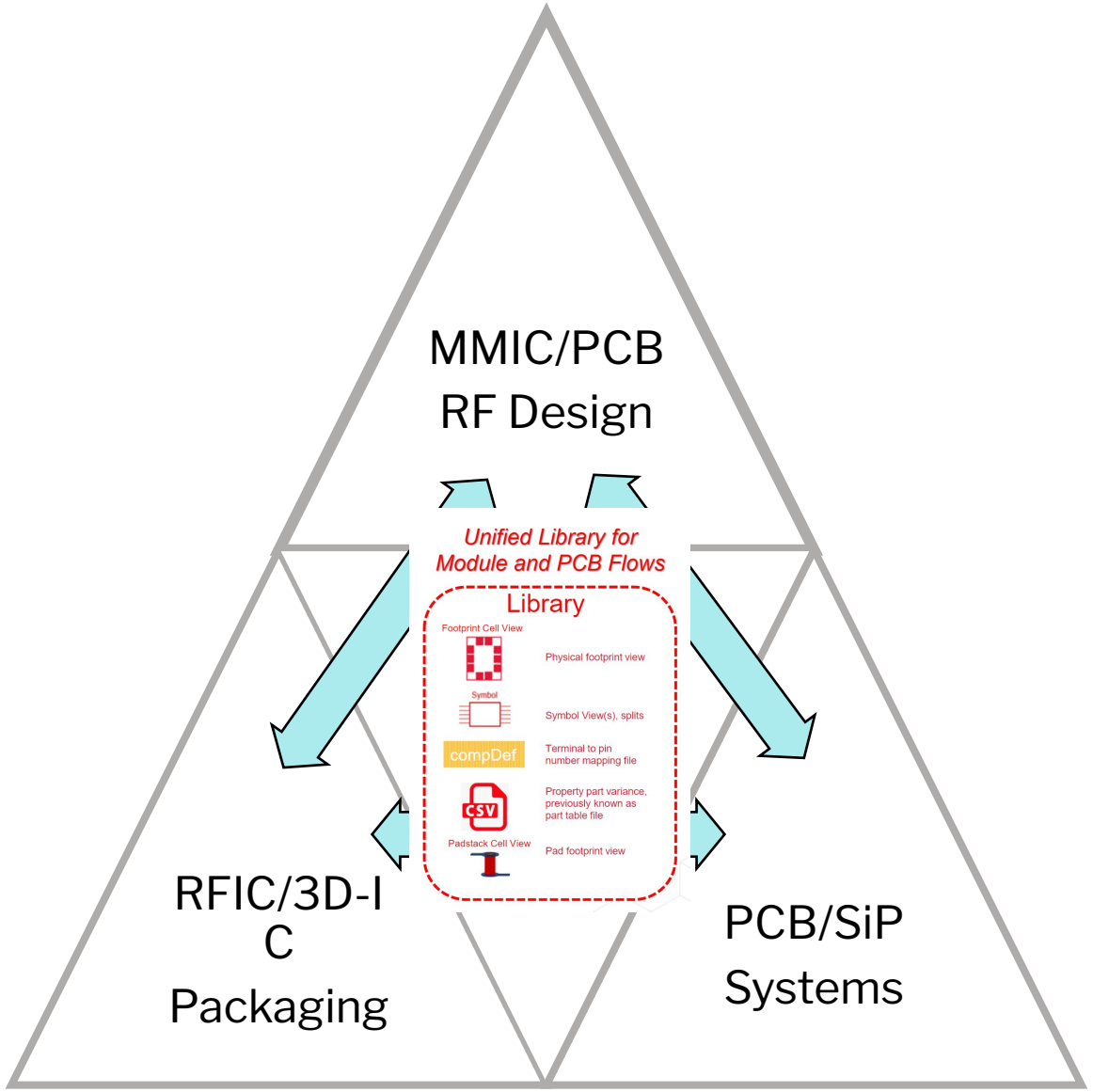
Analog/RF Co-Design and Co-Analysis Flow



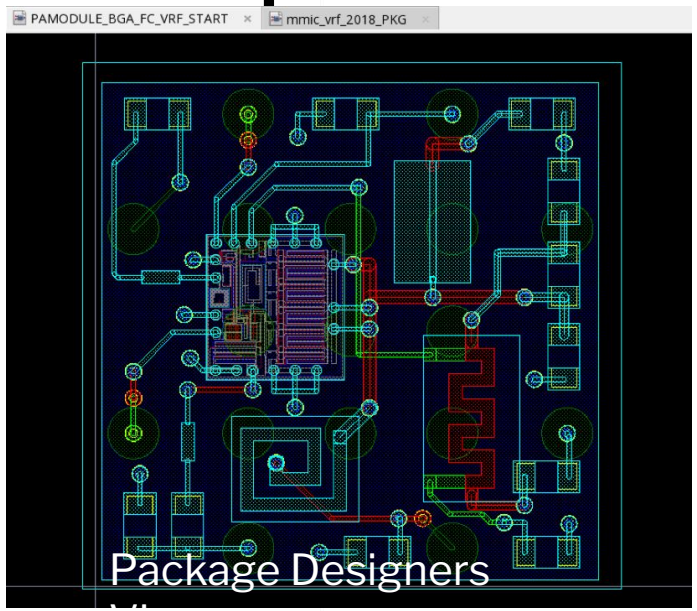
- Schematic-driven layout flow for die, chiplet, package and module design
- **Merged IC and package/module layout, to enable co-design** across multiple PDKs
- Smart electromagnetic and parasitic analysis, integrating multiple solver technologies
  - Geometry and mesh viewing
  - Automatic stitching of EM models into golden schematic
- Functional circuit simulation with embedded on-die and off-die layout parasitics
- Physical verification and manufacturing outputs

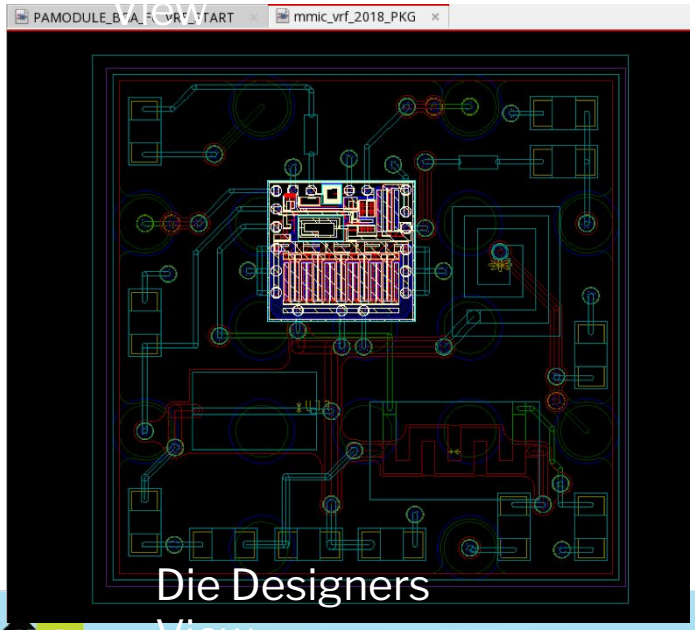
Unified Library is Central to Co-Optimization

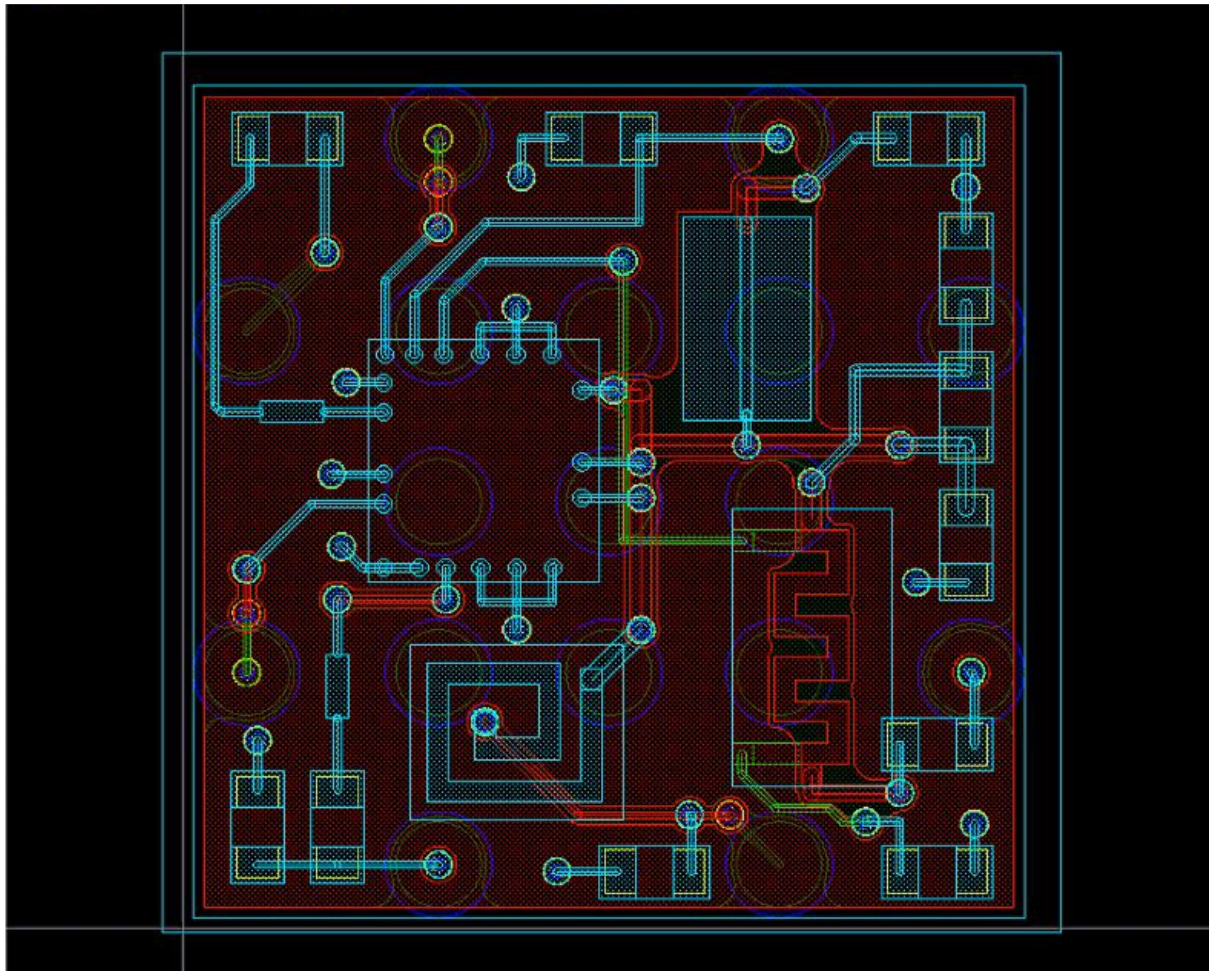
Central Unified Library management tools for all platforms



Example: IC/Package Co-Design

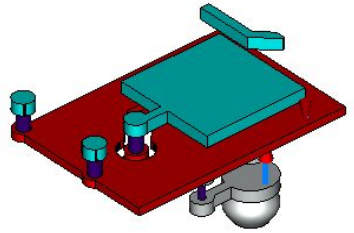




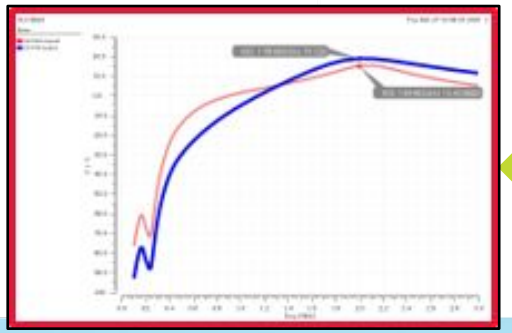


System-Level Layout Parasitic Back-Annotation and Simulation

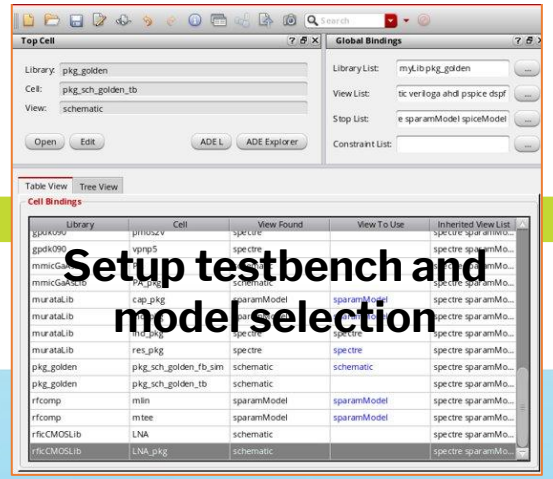
- Coupled 3D-EM extraction between chip(let), package, and PCB layout databases
  - Partial/full nets, groupings, and device-level modeling
  - S-parameters (freq. domain) and RLGC (time domain) models
- Automatically create schematics (extracted views) that include the layout parasitics from the package and PCB
  - Must support multi-PDK, multi-die solutions (namespace collision avoidance)



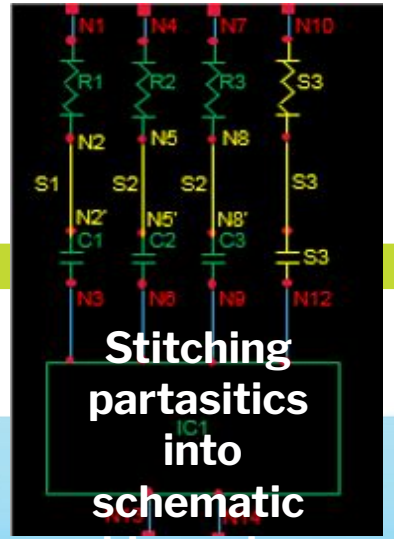
S-Parameter Model



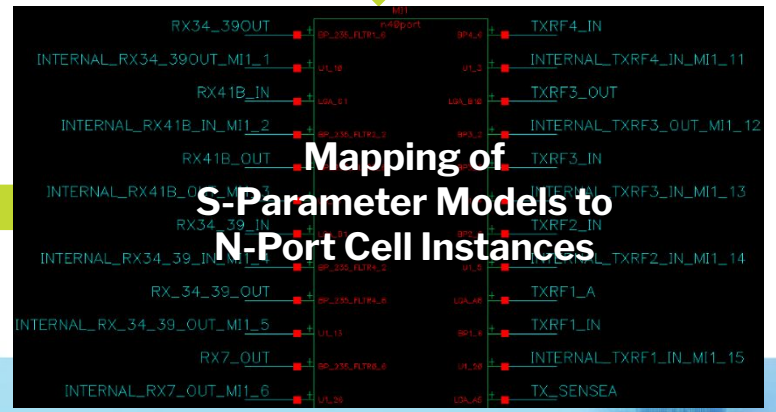
Simulate



Setup testbench and model selection



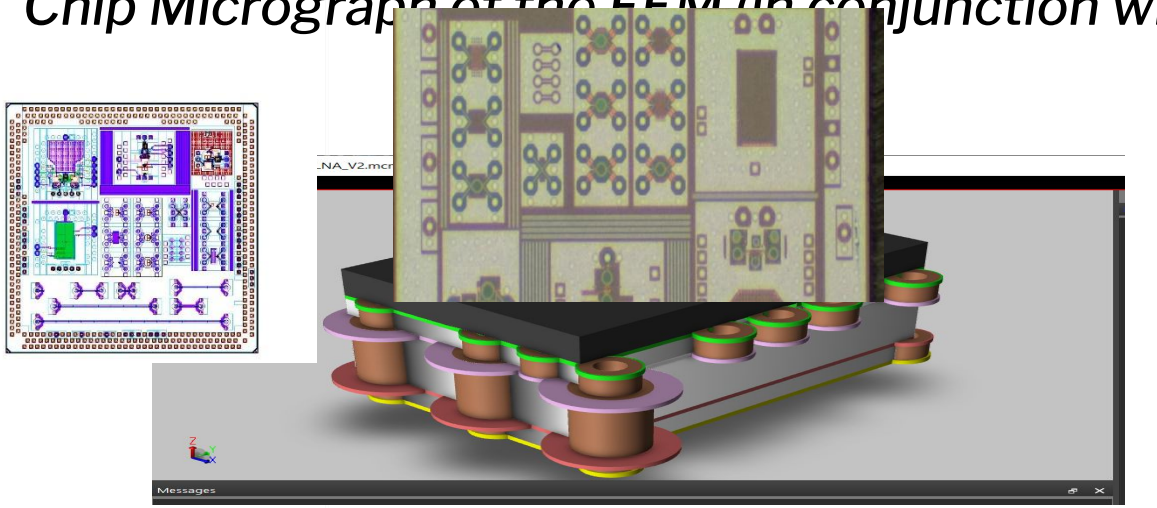
Stitching partasitics into schematic hierarchy



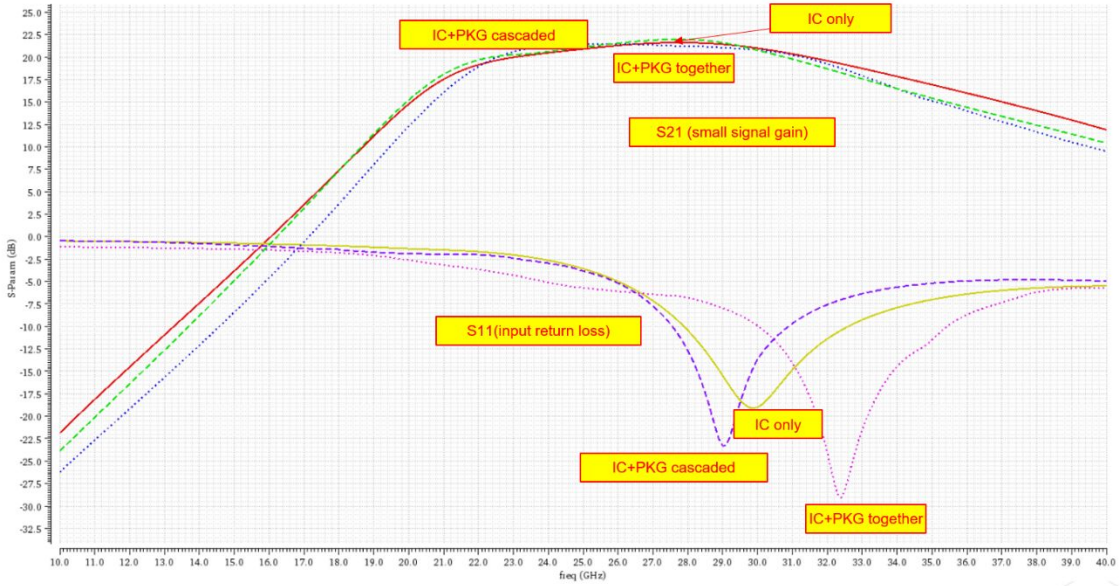
Mapping of S-Parameter Models to N-Port Cell Instances

Example: Co-Design/Analysis is essential for Accuracy at mmWave

Chip Micrograph of the FEM (in conjunction with test-package) and measured data



Power Amplifier Performance (Simulations)



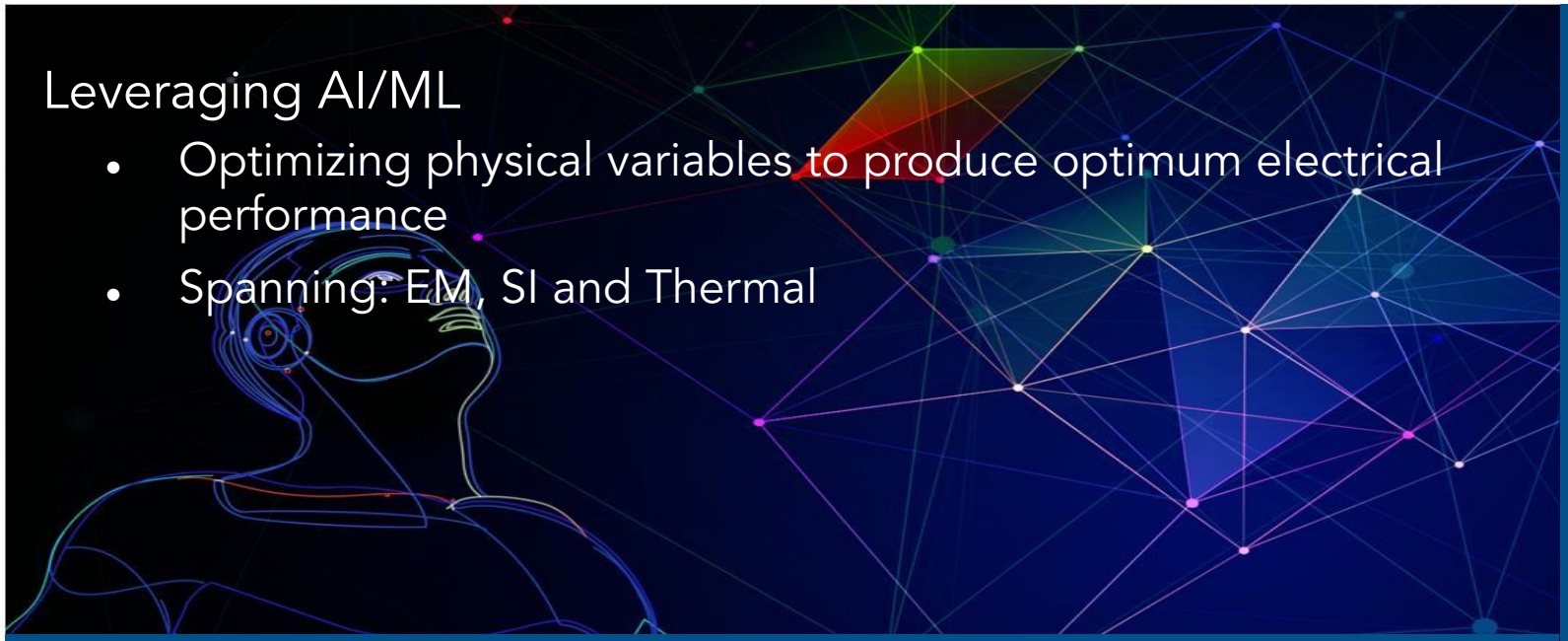
1. Die IO Co-design: Plan placement of IO and bumps on Die in context of surrounding package

2. Die-Package co-EM extraction. Extract Combined geometry to get the coupling effects
   a. Incrementally EM-extract and verify as you build

3. System Simulations
   a. Simulation IC functionality in context of Package/PCB parasitics

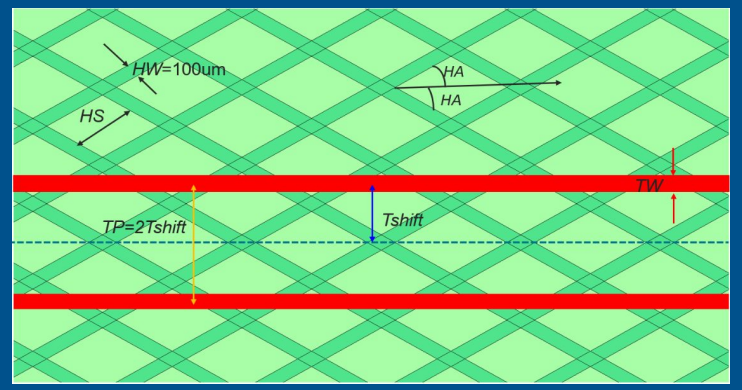
Unleashing AI for Package Optimization

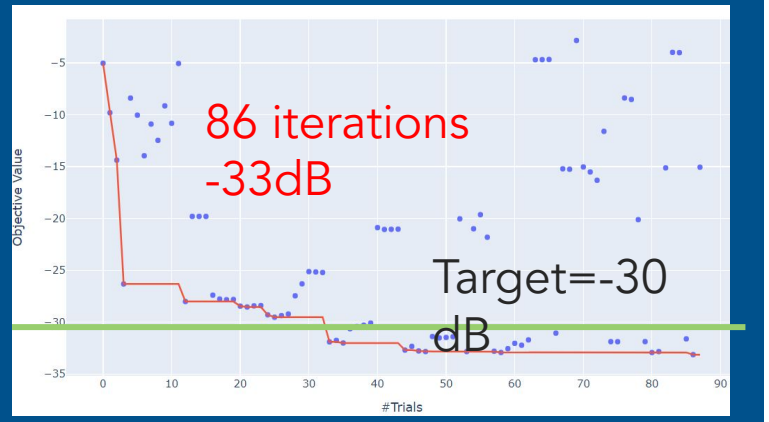
Enabling Automation and Optimization with Analysis Engines: Unlocking Best PPA



Leveraging AI/ML

- Optimizing physical variables to produce optimum electrical performance
- Spanning: EM, SI and Thermal





Example:

- Minimize transmission line return loss:
  - -30dB target in the frequency band [0GHz-15GHz]
- 5 physical variables: *HW, HS, HA, TW, TP*
- Brute-force sweeping requires 2,880,000 evaluations (20x20x18x20x20)

Layer Icon	Layer Name	Thickness(mm)	Material	Er	Loss Tangent
	Plane_cross_hatch_L4	0.0175	COPPER	3.1	0.024
	Medium01	0.03		2.8	0.024
	Signal_Differential_L5	0.0175	COPPER	2.8	0.024
	Medium02	0.03		2.8	0.024
	Plane02_cross_hatch_L6	0.0175	COPPER	3.1	0.024

Conclusion

- **The age of Moore-than-Moore has arrived, and advanced packaging is central**
- **There are still many challenges to overcome to bring 3D heterogeneous integration to the mainstream**
- **The worlds of IC designers and package designers are converging**
- **IC/package/PCB co-design and analysis are necessary**
- **Co-Design environment is essential for the best QoR and TAT**